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Patentanmeldung Nr. Patent application No. Demande de brevet n°

00403280.1

Der Präsident des Europäischen Patentamts;  
Im Auftrag

For the President of the European Patent Office

Le Président de l'Office européen des brevets  
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**Blatt 2 der Besch inigung**  
**Sheet 2 of the certificate**  
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## APPARATUS AND METHOD FOR CONTROLLING A POWER SUPPLY

## FIELD OF THE INVENTION

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The present invention relates in general to a power supply and more particularly, though not exclusively, to an apparatus and method for controlling a power supply by applying a temporary load to the power supply in order to generate a control signal.

## BACKGROUND OF THE INVENTION

15 Dual switched-mode power supplies are commonly used for electronic devices such as televisions that generally operate at two power levels, a high power level during normal operation and a low power level during standby operation. For example, for a television the high power level corresponds to providing power to the picture tube, receiver, speaker, and control circuitry, and the low power level corresponds to supplying power only to the control circuitry so that the television remains in a standby mode. A large, main switched-mode power supply is used to provide power to the picture tube, receiver, and speaker, and a small, auxiliary switched-mode power supply is used to supply power to the control circuitry.

25 The control circuitry for the television generally comprises a microprocessor to control the various functions of the television, memory to store operating information like the last volume level and last channel watched by the user, and a detector to receive signals

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from a remote control unit. The use of the dual power supply conserves energy when the television is in the standby mode.

To operate the television, the user generally  
5 presses a button on the remote control, which transmits a signal to the detector in the television. The detector transmits the signal to the microprocessor, which decodes the signal and performs the requested function, for example, turning on or off the television.

10 When the user has requested that the television turn off, the microprocessor turns off the main power supply, leaving the auxiliary power supply on. In prior televisions, because the control circuitry is located on the isolated side of the auxiliary power supply, complex  
15 circuitry such as a mechanical relay or a combination of signals on a secondary-side optocoupler, which provides a normal feedback plus a forced standby signal in response to the user requesting the shutdown of the television, is used to communicate the shutdown command from the control  
20 circuitry to the main power supply. It would be desirable to communicate this command using simplified circuitry. Accordingly, it would be advantageous for an improved dual power supply configuration to communicate a shutdown command to the main power supply  
25 from control circuitry powered by the auxiliary power supply.

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## BRIEF SUMMARY OF THE INVENTION

Therefore, in a first aspect, the invention  
5 provides a control circuit for controlling a first  
power supply, comprising: an input for coupling to a  
temporary load; and an output for coupling to a second  
power supply wherein, in response to the coupling to  
the temporary load for a predetermined time period, a  
10 signal is provided to control the second power supply.

According to a second aspect, the invention  
provides a control circuit for controlling a first  
power supply, comprising: a first control input for  
receiving a feedback signal; a first comparator for  
15 generating, responsive to the feedback signal, a  
compare signal having a first state and a second state;  
and a first control output for providing a control  
signal to a second power supply, wherein the control  
signal changes state in response to the compare signal  
20 being in the first state for a time period exceeding a  
reference time period.

In a third aspect, the invention provides a dual  
power supply, comprising: a first power supply  
comprising a control circuit and a power circuit,  
25 wherein the power circuit has an output for coupling to  
a temporary load; a second power supply coupled to an  
output of the control circuit; and wherein the control  
circuit generates a signal to control the second power  
supply in response to the coupling to the temporary  
30 load for a time period that exceeds a reference time  
period.

According to a fourth aspect, the invention  
provides a method of operating a dual power supply,  
wherein the dual power supply comprises a first power

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supply and a second power supply, comprising: coupling  
a temporary load to an output of the first power  
supply; and responsive to the coupling of the temporary  
load for a predetermined time, providing a signal to  
5 the second power supply for switching the second power  
supply on and off.

In a fifth aspect, the invention provides a  
control circuit for providing a control signal, the  
control circuit comprising a timer circuit having an  
10 input for receiving an input signal corresponding to a  
temporary load state and having an output for  
providing, in response to receiving the input signal  
for a predetermined time period, the control signal.

15

#### BRIEF DESCRIPTION OF THE DRAWINGS

Embodiments of the invention will now be more fully  
described, by way of example, with reference to the  
20 drawings, of which:-

FIG. 1 is a schematic diagram of a dual power  
supply, having an auxiliary power supply powering a  
control load, according to an embodiment of the present  
25 invention;



FIG. 2 is a schematic diagram illustrating the application of a temporary load to the auxiliary power supply of FIG. 1 according to an embodiment of the present invention;

5 FIG. 3 is a more detailed schematic diagram of the auxiliary power supply of FIG. 2;

FIG. 4 is a schematic diagram of a timer circuit for the auxiliary power supply of FIG. 3;

10 FIG. 5 is a voltage waveform illustrating normal operation of the dual power supply of FIG. 2; and

FIGs. 6 and 7 are voltage waveforms illustrating operation of the dual power supply of FIG. 2 after application of the temporary load.

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#### DETAIL DESCRIPTION OF THE DRAWINGS

20 FIG. 1 is a schematic diagram of a dual power supply 100 comprising an auxiliary power supply 102 that provides power to a control load 104. A main power supply 106 provides power to a main load 108. A MAINS input terminal 101 provides, for example, AC power to auxiliary  
25 power supply 102 and main power supply 106. Main load 108 and control load 104 correspond, for example, to the power loads of a television or other electronic device. Main load 108 includes, for example, a picture tube, and control load 104 includes, for example, control circuitry  
30 for the television such as a microprocessor and memory. As discussed further below, the microprocessor is used to

communicate operating information, for example commands from a user to turn on or off the electronic device, to the auxiliary power supply.

FIG. 2 is a schematic diagram illustrating the application of a temporary load 204 to auxiliary power supply 102 of FIG. 1 according to an embodiment of the present invention. Auxiliary power supply comprises a power circuit 200, a feedback circuit 202, and a control circuit 203. Auxiliary power supply 102 is, for example, a switched-mode power supply.

Temporary load 204 is, for example, a resistive load coupled to temporarily overload auxiliary power supply 102. In response to the application of temporary load 204, control circuit 203 provides a control signal STANDBY to main power supply 106. The STANDBY signal generally alternates between two states, an on state and an off state, used to control main power supply 106 on and off.

FIG. 3 is a more detailed schematic diagram of power circuit 200, feedback circuit 202, and control circuit 203 and the external circuit connections of auxiliary power supply 102. Power circuit 200 receives a voltage  $V_{in}$  from MAINS input terminal 101 that is coupled to the primary side of transformer T. A switching power transistor M1 is coupled to control primary current through transformer T. Transistor M1 is, for example, an N-type MOSFET. A resistor  $R_{sense}$  is coupled in series with transistor M1 to provide a voltage  $V_{sense}$  to control circuit 203 that is indicative of the primary current flow through transformer T.

The secondary side of transformer T is coupled to a diode D1 and output supply capacitor  $C_{out}$  to provide a rectified voltage  $V_{out}$  at output node 306 to control load

104, which is represented generally by resistive load  $R_{load}$ . Temporary load 204 is coupled to output node 306 and comprises, for example, a resistor  $R1$  coupled in series with a switch  $S1$ . A switching voltage input  $V_{S1}$  controls switch  $S1$  and is provided, for example, by a microprocessor (not shown) in the control circuitry of control load 104. Switch  $S1$  may be, for example, a relay, a MOSFET, or a bipolar transistor. In addition to the above approach, other ways of temporarily overloading auxiliary power supply include the unbalancing of feedback circuit 202 by using a switch in feedback circuit 202 (for example, implemented in silicon or by mechanical means) so that auxiliary power supply 102 responds as if in an overloaded condition.

Feedback circuit 202 has an input coupled to node 306 and comprises, for example, a voltage divider provided by resistors  $R2$  and  $R3$  connected in series. The output voltage  $V_{divider}$  from the voltage divider is provided as a feedback signal to control circuit 203.

Control circuit 203 comprises a comparator 302 having an inverting input for receiving the feedback signal from feedback circuit 202. Comparator 302 is a hysteretic comparator. A non-inverting input of comparator 302 is coupled to a voltage reference  $V_{ref1}$ .

Comparator 302 provides an output signal  $CMP$  that controls the charging and discharging cycle of power circuit 200. During normal operation,  $CMP$  generally alternates between two states, an on state authorizing the primary power cycling and an off state preventing the cycling of power circuit 200. When  $CMP$  is in an on state (i.e. a logic high state), transistor  $M1$  may be turned on

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at a rate dictated by the oscillator. When CMP is in an off state (i.e. a logic low state), transistor M1 cannot be activated at all.

A logical AND gate A1 has an input to receive signal  
5 CMP and an input to receive a data output signal Q from a latch LATCH1, such as for example an S-R type latch configured as illustrated. The output of gate A1 is coupled to a control terminal of transistor M1 to control current flow through the primary side of power circuit  
10 200.

A comparator 304 has a non-inverting input coupled to receive voltage  $V_{sense}$  and an inverting input coupled to a voltage source  $V_{over\_I}$ . The output of comparator 304 is coupled to the reset input of LATCH1. An oscillator  
15 signal is coupled to the set input of LATCH1.

During operation, when signal CMP is in a high state, each time the OSCILLATOR signal activates LATCH1 and the Q output goes high, transistor M1 turns on and current builds up in the primary inductance of  
20 transformer T. D1 does not yet conduct current because of the dot windings configuration of transformer T as shown in FIG. 3. Comparator 304 monitors the current build-up and resets LATCH1 so that transistor M1 turns off. Specifically, voltage  $V_{sense}$  increases until it  
25 exceeds  $V_{over\_I}$ , at which point the output of comparator 304 goes high and resets LATCH1. In response to transistor M1 turning off, the voltage of the transformer T primary inductance reverses and energy transfer now takes place in the secondary transformer inductance.  
30 Voltage  $V_{out}$  increases by one step due to current conduction through D1. A new switching cycle occurs, and  $V_{out}$  rises by additional steps for as long as CMP remains in an on state. Referring to FIG. 5, which is discussed

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in more detail below, when  $V_{out}$  has reached the upper voltage threshold LEVEL1 indicated in FIG. 5, CMP goes low, turns off transistor M1, and  $V_{out}$  slowly decreases with a slope determined by  $C_{out}$  and  $R_{load}$ . When  $V_{out}$  has  
5 reached the lower voltage threshold LEVEL2, CMP goes high again and a new cycle occurs.

### Timer Circuit

A timer circuit 300 receives signal CMP and provides  
10 control signal STANDBY to main power supply 106. When temporary load 204 is applied to output node 306 by switch S1 such that the auxiliary supply is overloaded, signal CMP goes to a high state for as long as temporary load 204 is applied. Because of the length of time that  
15 temporary load 204 is applied, signal CMP remains in this high state for a period of time that is greater than the time period during normal operation prior to applying temporary load 204. Timer circuit 300 monitors the time period that CMP is in a high state and triggers a change  
20 in the state of the STANDBY signal in response to this time period exceeding a reference time period determined by timer circuit 300, as discussed further below. If the time period does not exceed the reference time period, then the signal STANDBY remains unchanged. The  
25 comparison to the reference time period protects against providing an incorrect STANDBY signal, for example caused by spurious voltage variations in auxiliary power supply 102.

FIG. 4 is a schematic diagram of timer circuit 300  
30 according to one specific approach. A comparator 400 has a non-inverting input coupled to resistor R4, capacitor C1, and diode D2, and an inverting input coupled to a voltage reference source  $V_{ref2}$ . R4 and C1 provide an RC

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time constant used to establish the reference time period mentioned above. The output of comparator 400 provides a signal GTS and is coupled to a latch LATCH2, which may be for example a D-type latch configured as shown. However, 5 other types of latches and timers may be used in other embodiments. LATCH2 has a clock input for receiving the output of comparator 400 and a data output Q for providing the signal STANDBY. The inverse data output  $\bar{Q}$  of LATCH2 is coupled to the data input D, and the set 10 and reset inputs are tied to ground.

#### Waveform

FIG. 5 is a voltage waveform illustrating normal operation of dual power supply 100. Specifically, 15 voltage  $V_{out}$  is illustrated versus time and varies between voltages LEVEL1 and LEVEL2. The average voltage  $V_{out\_avg}$  of  $V_{out}$  is also shown. Signal CMP is also shown. When CMP is in an on or high state,  $V_{out}$  is increasing with a ripple voltage 500 due to the switched-mode 20 characteristics of auxiliary power supply 102. When CMP is in an off state,  $V_{out}$  is decreasing since transistor M1 is turned off and control load 104 discharges supply output node 306.

Signal CMP is a feedback signal responsive to the 25 power being delivered to control load 104. As the load varies, the time period of the on and off states of CMP varies to keep  $V_{out\_avg}$  substantially constant. More specifically, and referring again to FIG. 3, CMP varies in response to the voltage  $V_{out}$ . When  $V_{out}$  is at LEVEL2, 30 voltage  $V_{divider}$  is at a low level less than voltage  $V_{ref1}$ . Thus, CMP goes to a high level or on state, which enables transistor M1 to turn on to permit charging by power circuit 200 and to provide an increasing voltage  $V_{out}$ .

$V_{out}$  continues to increase until reaching LEVEL1, at which point  $V_{divider}$  is at a high level greater than  $V_{ref1}$ . Thus, CMP goes to a low level or off state. It should be noted that due to the nature of hysteretic comparator

5 302,  $V_{ref1}$  will have a value that is different depending on whether  $V_{divider}$  is rising or falling. This hysteresis simply provides two different levels (LEVEL1 and LEVEL2 as indicated in FIG. 5) necessary to the power supply operating mode (this type of supply is sometimes also

10 referred to as a ripple-mode switched-mode power supply). The cycle repeats itself once  $V_{out}$  again reaches LEVEL2.  $V_{ref1}$  is set to an appropriate value between LEVEL1 and LEVEL2 using standard techniques appropriate for this type of power supply.

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#### Controlling the Main Power Supply

When a user of an electronic appliance, such as for example a television, decides to turn it off (or alternatively, when another electronic system or circuit

20 sends a shutdown signal to dual power supply 100), the user activates a remote control to send (or the other system or circuit sends) a signal, which is decoded by a microprocessor in the control circuitry for the television. The microprocessor asserts  $V_{s1}$  to turn on

25 switch S1 to connect temporary load 204 to the output of power circuit 200 for a time period programmed into the microprocessor or otherwise predetermined and fixed. After this predetermined time period has passed, then  $V_{s1}$  is no longer asserted, and switch S1 is opened.

30 In response to the application of the temporary load for this predetermined time period, voltage  $V_{out}$  decreases and lowers  $V_{divider}$  below  $V_{ref1}$  so that CMP goes to an on

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state. If CMP remains at this on state for a sufficient time, then timer circuit 300 asserts STANDBY to turn off main power supply 106.

More specifically, each time that signal CMP goes to  
5 a high level, timer circuit 300 monitors the time that CMP remains at the high level. This monitoring is continuously done both during normal operation and otherwise. Referring again to FIG. 4, when CMP is high, C1 is charged through R4. If CMP is high for a time  
10 period sufficient for C1 to charge to a voltage greater than  $V_{ref2}$ , then GTS goes high. However, during normal operation, CMP goes low during each charging cycle before C1 is sufficiently charged to trigger a change in GTS, and accordingly, GTS remains at a low state or off state  
15 corresponding, for example, to normal operation of a television. When CMP returns to a low level, C1 is discharged through diode D2 in preparation for the next time that CMP again goes high.

LATCH2 provides control signal STANDBY and toggles  
20 STANDBY between an on state (corresponding to a standby or shutdown mode) and an off state (corresponding to normal operation) each time that GTS goes to an ON state. Thus, when CMP is at a high state for a time period greater than the reference time period established by R4  
25 and C1 and the comparison voltage value provided by  $V_{ref2}$ , then GTS goes high, which latches STANDBY to a high state and turns off main power supply 106.

To turn, for example, the television on again, the user again activates the remote control, which in turn is  
30 decoded by the microprocessor in the control circuitry to again assert  $V_{s1}$  and apply the temporary load to the output of power circuit 200 for another predetermined time, for example the same time period used to initiate



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shut-down. As described above,  $V_{out}$  again falls and  $V_{divider}$  falls below  $V_{ref1}$ , so that CMP goes high. Timer circuit 300 again monitors the time that CMP is in this high state, and comparator 400 asserts GTS to latch  
5 STANDBY to an off state so that the main power supply 106 turns on again.

FIGs. 6 and 7 are voltage waveforms illustrating the operation of dual power supply 100 after application of temporary load 204 to auxiliary power supply 102. In  
10 FIG. 6, switch S1 is closed at a point indicated by reference numeral 600. CMP was high prior to switch S1 closing and remains in a high state, indicated by reference numeral 602, for a time period 604 sufficient to trigger timer circuit 300. Then, GTS goes high at a  
15 point as indicated by reference numeral 606.

In FIG. 7, the user requests the turn-off of, for example, the television at point 700. Switch S1 is closed, and CMP remains at a high state for a sufficient time for STANDBY to be latched to a high or on state,  
20 which turns off main power supply 106. At point 702, switch S1 is turned off.

At point 704, the user requests that the television be turned on and switch S1 is again turned on for a predetermined time period. CMP remains high for a  
25 sufficient time that STANDBY is latched to a low or off state so that main power supply 106 is turned on.

#### Advantages

By the foregoing description, a novel and  
30 unobvious apparatus and method for controlling a power supply have been disclosed. The described embodiments have the advantages of providing simplified circuitry for communicating a shutdown command from control circuitry power by an

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auxiliary power supply to the main power supply. For example, it is not necessary to use an optocoupler in this communication as with prior dual power supplies. It is also possible to use a fully primary regulated auxiliary power supply where no optocoupler is implemented. In addition, overall standby power is not degraded since switch S1 is relaxed to remove the temporary load and the STANDBY signal is latched to maintain the shutdown state of the main power supply.

Although specific embodiments have been described above, numerous modifications and substitutions may be made thereto without departing from the spirit of the invention. For example, while the description above is discussed specifically in the context of an AC-DC converter, other power supply configurations may be used with the present invention including DC-DC converters. Also, the present invention may also be used with other electronic devices using two or more power supplies. Accordingly, the invention has been described by way of illustration rather than limitation.

Alternative embodiments of the invention can be implemented as a computer program product for use with a computer system, the computer program product being, for example, a series of computer instructions stored on a tangible data recording medium, such as a diskette, CD-ROM, ROM, or fixed disk, or embodied in a computer data signal, the signal being transmitted over a tangible medium or a wireless medium, for example microwave or infrared. The series of computer instructions can constitute all or part of the functionality described above, and can also be stored in any memory device, volatile or non-volatile, such as semiconductor, magnetic, optical or other memory device.

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CLAIMS

1. A control circuit for controlling a first power supply, comprising:

5       an input for coupling to a temporary load; and  
      an output for coupling to a second power supply  
wherein, in response to the coupling to the temporary load for a predetermined time period, a signal is provided to control the second power supply.

10

2. The control circuit of claim 1 wherein the input of the control circuit is coupled to the temporary load through a feedback circuit.

15 3. The control circuit of claim 1 further comprising a comparator having an output coupled to generate the signal to control the second power supply, wherein:  
the first power supply provides an output supply voltage;  
the output of the comparator varies alternately  
20 between an on state corresponding to an increasing output supply voltage and an off state corresponding to a decreasing output supply voltage;

the on state corresponds to a first time period prior to the coupling to the temporary load;

25       in response to the coupling to the temporary load, the output of the comparator goes to the on state for a second time period greater than the first time period;  
and

30       in response to the output of the comparator going to the on state for the second time period, the signal is provided to the second power supply.

4. The control circuit of claim 3 wherein the predetermined time period is greater than the first time period.

5 5. The control circuit of claim 3 wherein the comparator is a hysteretic comparator.

6. The control circuit of claim 3 further comprising a timer circuit having an input coupled to the output of  
10 the comparator and having an output for providing the signal to control the second power supply in response to the second time period exceeding a reference time period.

7. The control circuit of claim 6 wherein the average  
15 power output of the first power supply is less than the average power output of the second power supply.

8. The control circuit of claim 6 wherein the signal is used to turn the second power supply on and off.

20

9. A control circuit for controlling a first power supply, comprising:

a first control input for receiving a feedback signal;

25 a first comparator for generating, responsive to the feedback signal, a compare signal having a first state and a second state; and

a first control output for providing a control signal to a second power supply, wherein the control  
30 signal changes state in response to the compare signal being in the first state for a time period exceeding a reference time period.

10. The control circuit of claim 9 further comprising:  
a feedback circuit having an output for providing  
the feedback signal;

a second control input for coupling to a power  
5 circuit to receive a signal indicative of the current  
supplied to the power circuit, wherein an output of the  
power circuit is coupled to an input of the feedback  
circuit; and

a second control output for coupling to the power  
10 circuit to control the current supplied to the power  
circuit.

11. The control circuit of claim 10 further comprising:

a logic gate having a first input coupled to an  
15 output of the first comparator and having an output  
coupled to the second control output of the control  
circuit; and

a timer circuit having an input coupled to the  
output of the first comparator and an output coupled to  
20 the first control output of the control circuit.

12. The control circuit of claim 11 wherein:

the feedback circuit further comprises a voltage  
divider; and

25 the power circuit further comprises:

a transformer having a primary side  
coupled to the second control input of the  
control circuit and a secondary side coupled to  
the output of the power circuit; and

30 a transistor having a control electrode  
coupled to the second control output of the  
control circuit and having a current electrode  
coupled to the primary side of the transformer.

13. The control circuit of claim 11 further comprising:

a latch having an output coupled to a second input of the logic gate, a first input coupled to an

5 oscillator, and a second input coupled to the second control input of the control circuit; and

a reference voltage coupled to a non-inverting input to the first comparator, wherein an inverting input to the first comparator is coupled to the first control

10 input of the control circuit.

14. The control circuit of claim 11 wherein the timer circuit comprises:

a second comparator;

15 a latch having an input coupled to an output of the second comparator and having an output for providing the control signal to the second power supply; and

a resistor and capacitor coupled to a non-inverting input of the second comparator for providing the

20 reference time period.

15. The control circuit of claim 10 wherein:

the output of the power circuit is coupled continuously to a control load;

25 the input of the feedback circuit is temporarily coupled to a temporary load for a predetermined time; and

the control signal is responsive to the feedback circuit being temporarily coupled to the temporary load.

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16. The control circuit of claim 15 wherein the temporary load is coupled to the feedback circuit by activating a switch coupled to the temporary load, wherein the switch comprises a control input for  
5 receiving a switching signal from control circuitry in the control load.

17. The control circuit of claim 16 wherein the control circuitry in the control load comprises a microprocessor  
10 having an output coupled to provide the switching signal.

18. The control circuit of claim 9 wherein the control signal is provided to a second power supply for switching the second power supply on and off.

15

19. A dual power supply, comprising:

a first power supply comprising a control circuit and a power circuit, wherein the power circuit has an output for coupling to a temporary load;

20 a second power supply coupled to an output of the control circuit; and

wherein the control circuit generates a signal to control the second power supply in response to the coupling to the temporary load for a time period that  
25 exceeds a reference time period.

20

20. The dual power supply of claim 19 wherein the control circuit comprises:

a hysteretic comparator having an input coupled to the output of the power circuit; and

5 a timer circuit having an input coupled to an output of the hysteretic comparator, wherein an output of the timer circuit provides the signal to control the second power supply.

10 21. A method of operating a dual power supply, wherein the dual power supply comprises a first power supply and a second power supply, comprising:

coupling a temporary load to an output of the first power supply; and

15 responsive to the coupling of the temporary load for a predetermined time, providing a signal to the second power supply for switching the second power supply on and off.

20 22. The method of claim 21 wherein providing the signal to the second power supply comprises:

detecting the coupling of the temporary load by monitoring a time period that an output from a comparator is in a first state, wherein the comparator has an input  
25 coupled to the output of the first power supply and wherein the output of the comparator alternates between a first state and a second state; and

providing the signal to the second power supply when the time period exceeds a reference time period.

30



23. The method of claim 22 wherein:

prior to coupling the temporary load, the voltage of the output of the first power supply rises and falls between a first level and a second level;

5 prior to coupling the temporary load, the first state of the output of the comparator corresponds to an increasing voltage at the output of the first power supply and the second state of the output of the comparator corresponds to a decreasing voltage at the  
10 output of the first power supply; and

after coupling the temporary load, the first state of the output of the comparator corresponds to a decreasing voltage at the output of the first power supply.

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24. The method of claim 23 wherein the signal to the second power supply is alternately latched between an on state and an off state; wherein the on state corresponds to turning on the second power supply and the off state  
20 corresponds to turning off the second power supply.

25. A method of operating a first power supply, comprising applying a temporary load to the first power supply to provide a signal for controlling a second power  
25 supply.

26. The method of claim 25 wherein the first power supply comprises a comparator and further comprising providing the signal to the second power supply  
30 responsive to an output of the comparator remaining in an on state longer than a reference time period.

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27. The method of claim 26 wherein the comparator is a hysteretic comparator.

28. The method of claim 26 comprising applying the  
5 temporary load for a predetermined time period.

29. The method of claim 25 wherein the signal is provided to shut down the second power supply.

10 30. A control circuit for providing a control signal, the control circuit comprising a timer circuit having an input for receiving an input signal corresponding to a temporary load state and having an output for providing, in response to receiving the input signal for a  
15 predetermined time period, the control signal.

31. The control circuit of claim 30 wherein:  
the input signal corresponds to a first power supply; and  
20 the control signal corresponds to a second power supply.

32. The control circuit of claim 31 wherein the temporary load state corresponds to a temporary coupling  
25 of a load to an output of the first power supply.

33. The control circuit of claim 30 further comprising a comparator having an output coupled to the input of the timer circuit.

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## 23

34. The control circuit of claim 33 wherein the output of the comparator varies alternately between an on state corresponding to an increasing output supply voltage of a first power supply and an off state corresponding to a  
5 decreasing output supply voltage of the first power supply;

the on state corresponds to a first time period prior to the receiving of the input signal;

in response to the receiving of the input signal,  
10 the output of the comparator goes to the on state for a second time period greater than the first time period;  
and

in response to the output of the comparator going to the on state for the second time period, the control  
15 signal is provided for turning off a second power supply.

35. A computer program element comprising computer program code means to make a processor execute a procedure to carry out the method of any one of claims  
20 21 to 29.

36. A computer program element according to claim 35, embodied on a computer readable medium.



## APPARATUS AND METHOD FOR CONTROLLING A POWER SUPPLY

## Abstract of the Disclosure

5        In a dual power supply, a main power supply is shut  
down by providing a signal from an auxiliary power  
supply. To generate the shutdown signal, a load is  
temporarily applied to the output of the auxiliary power  
supply for a predetermined time. The application of the  
10    load is detected using a hysteretic comparator in the  
auxiliary power supply that remains in a high state for a  
time period that exceeds a reference time period, which  
is established by a timer circuit. In response to  
exceeding the reference time period, the shutdown signal  
15    is sent to the main power supply.



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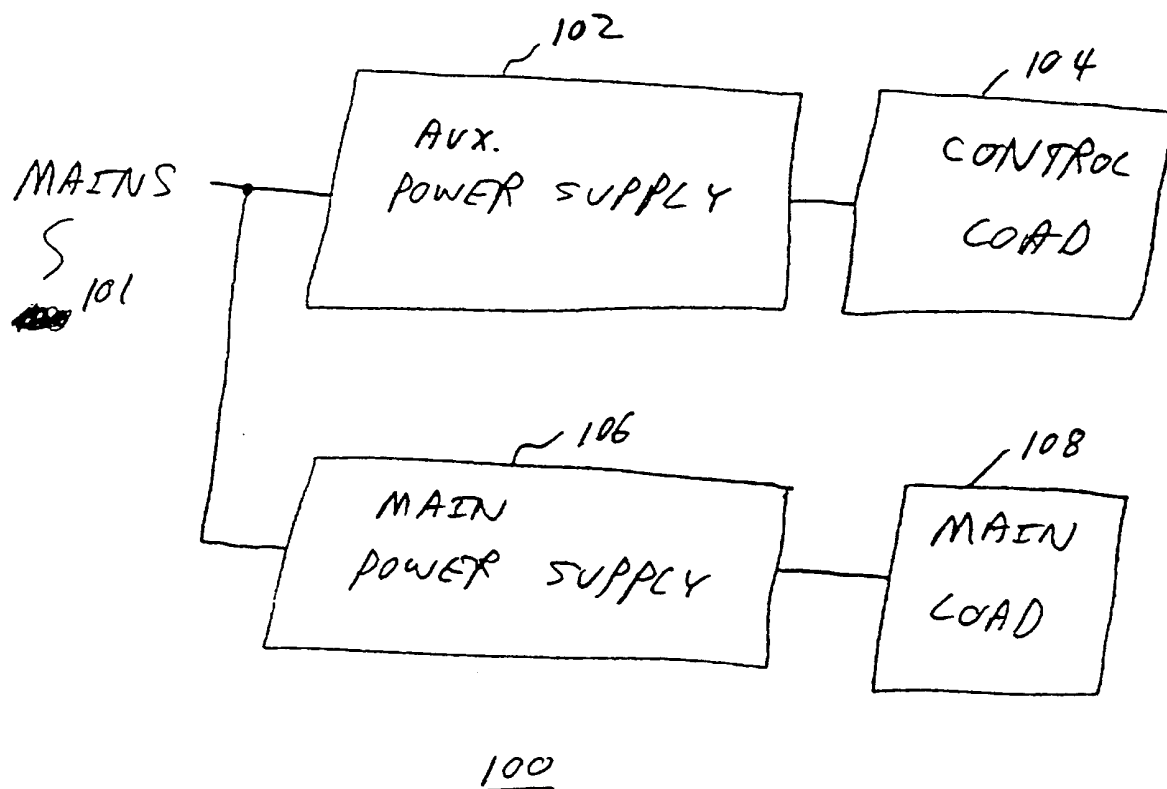


FIG. 1

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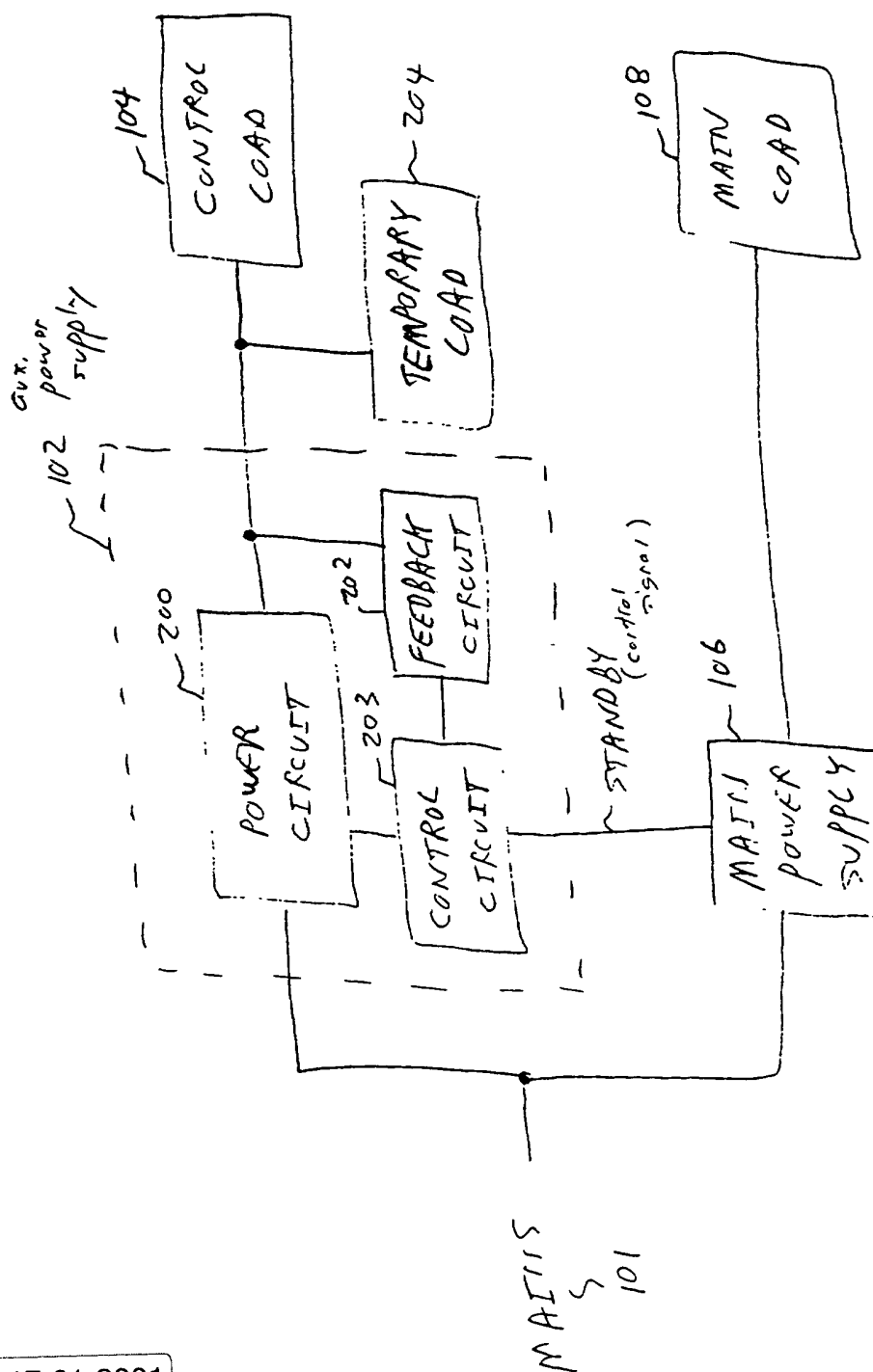


FIG. 2



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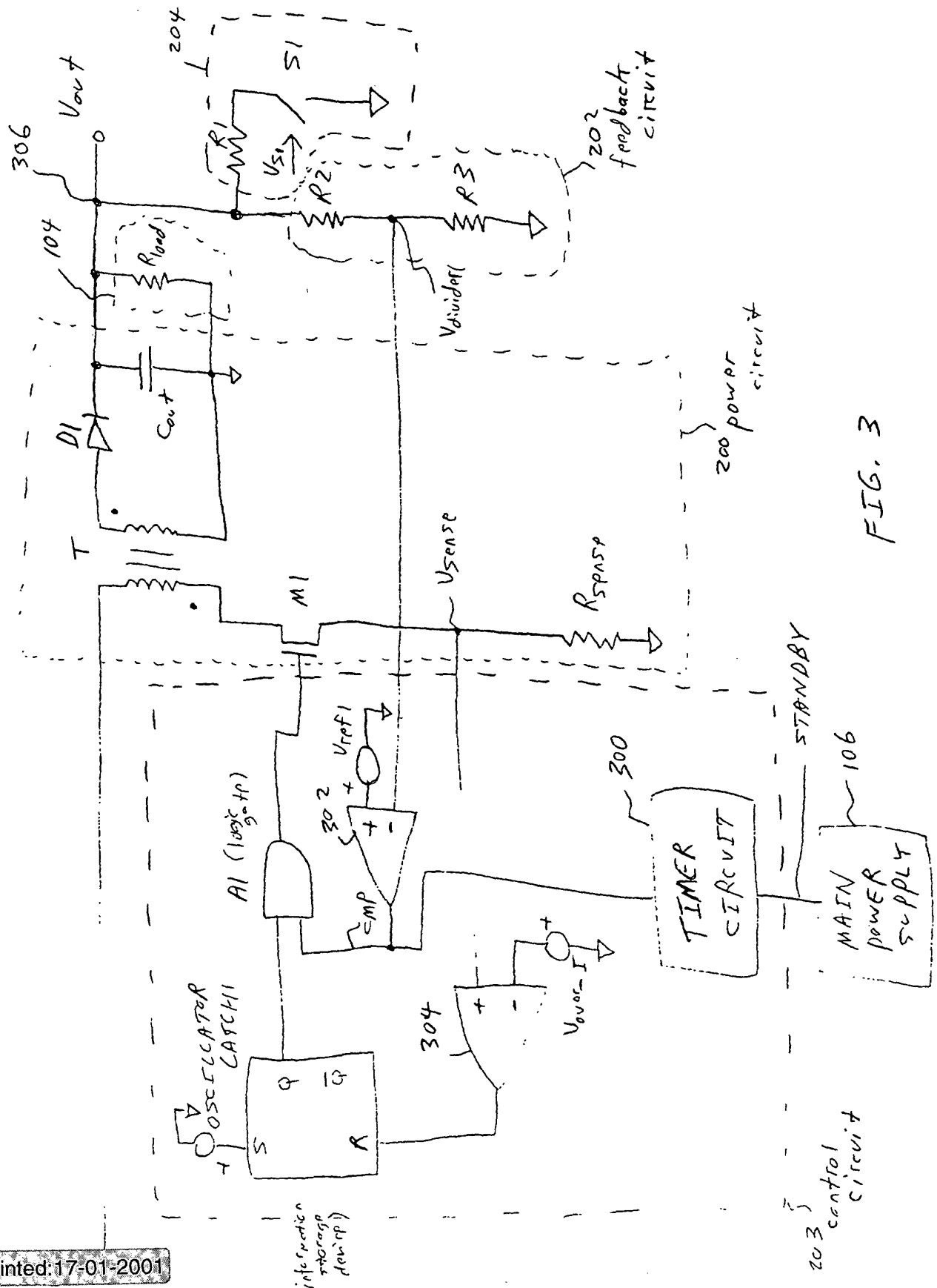


FIG. 3

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STANDBY

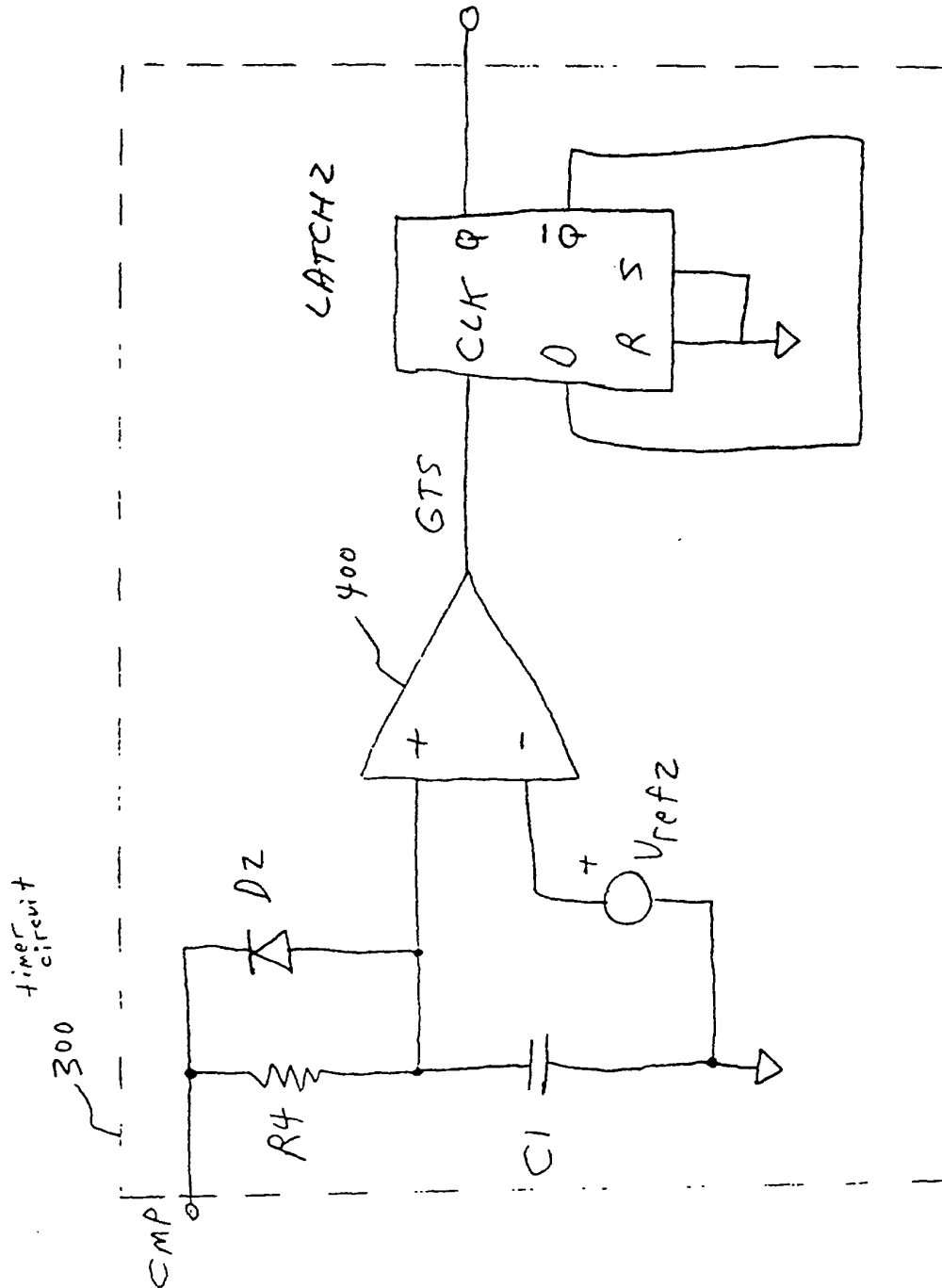


FIG. 4

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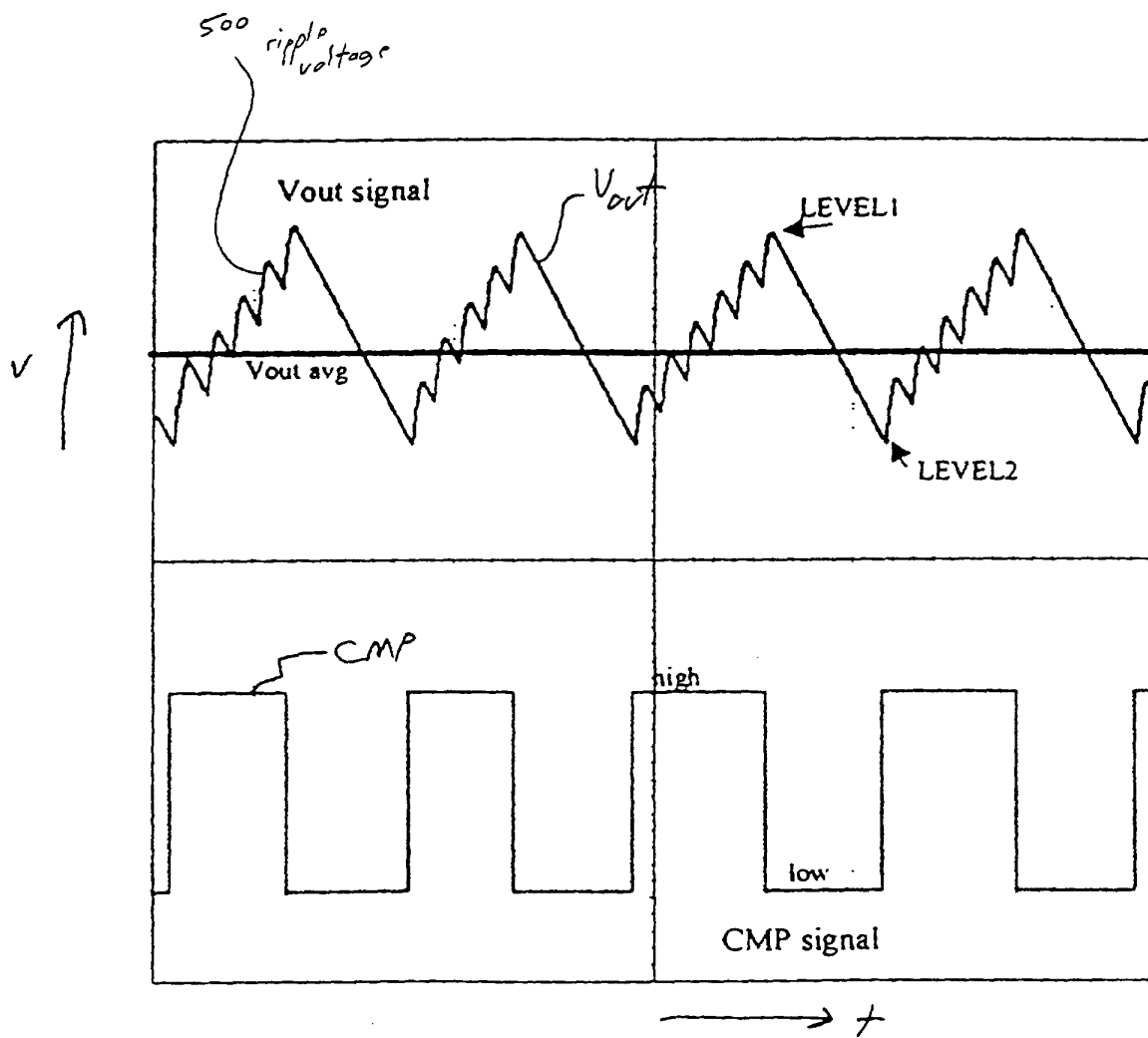


FIG. 5.

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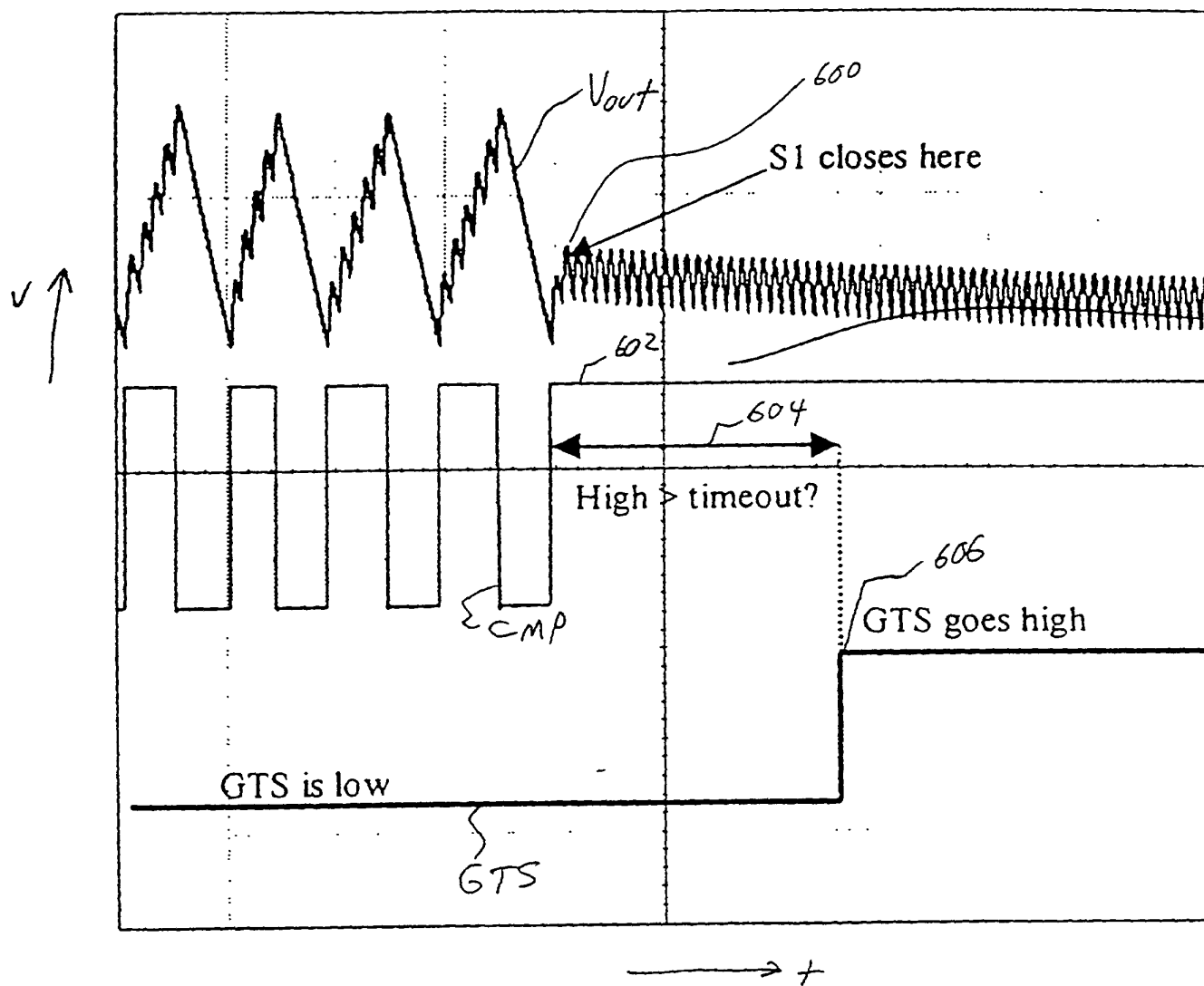


FIG. 6

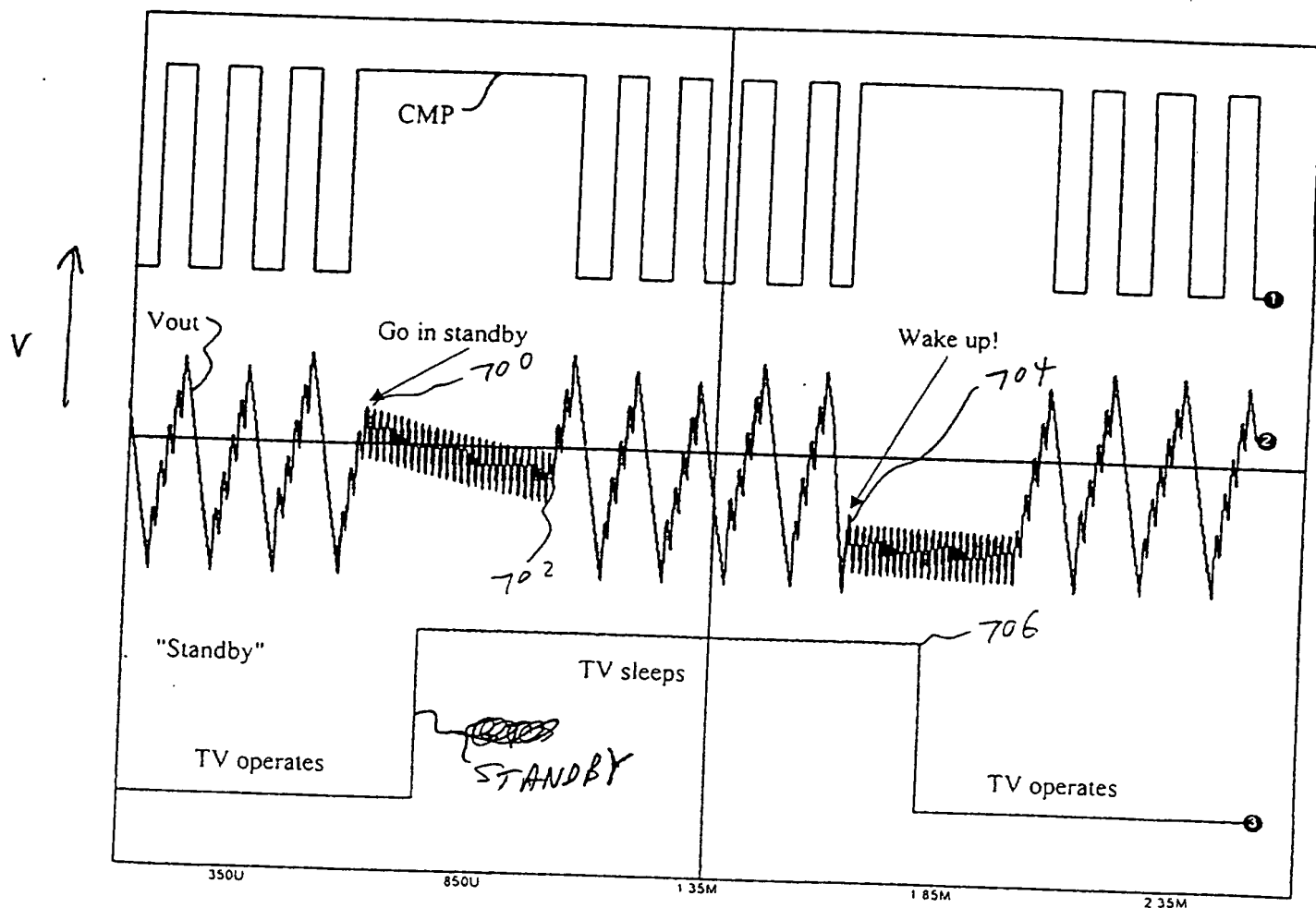


FIG. 7

